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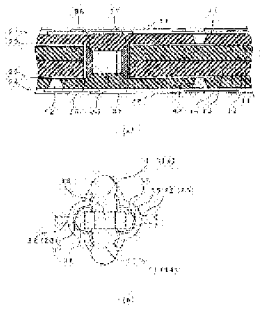
(54) WIRING BOARD INCORPORATING COMPONENT AND MANUFACTURING METHOD THEREOF



(57)Abstract:

PROBLEM TO BE SOLVED: To further improve component packaging density

without losing reliability in a wiring board for incorporating components and to provide its manufacturing method.

SOLUTION: First, a core-wiring board having a conductive layer at least on both upper and lower surfaces is manufactured, a through hole in which the cross section appearance consists of a plurality of arcs is formed on the core-wiring board that is manufactured so that space for positioning electric/electronic components to be incorporated is generated, the conductive layer is formed so that the inner surface of the formed through hole is included; the conductive layer on the upper and lower surfaces is subjected to patterning, the conductive layer formed at the through hole is divided according to the number of terminals of the electric/electronic components to be incorporated, the electric/electronic components are positioned in the space, the terminal of the positioned electric/electronic components and the divided conductive layer are connected by a conductive member, and then an insulating layer is laminated and formed overlapping on both the upper and lower surfaces of the core-wiring board, where the electric/electronic components are connected by the conductive wiring, so that the periphery of the electric/electronic components is filled.

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CLAIMS

[Claim(s)]

[Claim 1]

The process which manufactures the core patchboard which has a conductive layer to vertical both sides at least,

The process which forms the through tube to which a cross-section appearance becomes said manufactured core patchboard from two or more radii so that the space in which the electrical and electric equipment/electronic parts which should be built in should be located may be generated,

The process which forms a conductive layer so that the internal surface of said formed through tube may be included,

The process which carries out patterning of the conductive layer of said vertical both sides,

The process divided according to the number of the terminals of the electrical and electric equipment/electronic parts which should contain said conductive

layer formed in said through tube,
The process which locates the electrical and electric equipment/electronic parts in said space,
The process which connects said terminal and said divided conductive layer of said located electrical and electric equipment/electronic parts by the conductive member,
The process which carries out laminating formation of the insulating layer so that it may put on each of vertical both sides of said core patchboard to which said electrical and electric equipment/electronic parts were connected by said conductive member and may be filled up with the surroundings of said electrical and electric equipment/electronic parts
The manufacture approach of the patchboard with built-in components characterized by providing.
[Claim 2]
The manufacture approach of the patchboard according to claim 1 with built-in components characterized by having the process which forms the conductive layer from which said process which forms a conductive layer so that the internal surface of said formed through tube may be included serves as a substrate with nonelectrolytic plating, and the process which forms the conductive layer from which said formed substrate is used for a seed, and it becomes the upper layer with electrolysis plating.
[Claim 3]
The manufacture approach of a patchboard according to claim 1 with built-in components that said process which forms the through tube to which a cross-section appearance becomes said manufactured core patchboard from two or more radii so that the space in which the electrical and electric equipment/electronic parts which should be built in should be located may be generated is characterized by being made by drilling or metal mold punching.
[Claim 4]
The manufacture approach of the patchboard according to claim 1 with built-in

components characterized by for said process which locates the electrical and electric equipment/electronic parts in said space assigning supporter material to the bottom location of said core patchboard removed from said space, locating said electrical and electric equipment/electronic parts on said supporter material, and making it.

[Claim 5]

The manufacture approach of a patchboard according to claim 1 with built-in components that said process which connects said terminal and said divided conductive layer of said located electrical and electric equipment/electronic parts by the conductive member is characterized by using solder or conductive resin as said conductive member.

[Claim 6]

The manufacture approach of a patchboard according to claim 1 with built-in components that the process divided according to the number of the terminals of the electrical and electric equipment/electronic parts which should contain said conductive layer formed in said through tube is characterized by being made by drilling, metal mold punching, or laser beam machining.

[Claim 7]

The manufacture approach of claim 1 characterized by for said process which manufactures the core patchboard which has a conductive layer to vertical both sides at least manufacturing the core patchboard which has four wiring layers, and being manufactured so that the electrical installation of these wiring layers may be made by the conductive bump thru/or the patchboard with built-in components of six given in any 1 term.

[Claim 8]

The conductive layer which the cross-section configuration which was laid under the plate vertical side, without expressing, and was formed in the plate thickness direction becomes from two or more radii,

Electrical and electric equipment/electronic parts laid underground in the plate so that it might have a terminal and said terminal might counter said conductive

layer laid underground,
The connection member which connects said terminal and said conductive layer electrically and mechanically, without being prepared in the gap of said terminal and said conductive layer of said electrical and electric equipment/electronic parts laid underground, and contacting the longitudinal direction edge of said conductive layer,
The insulating layer of two upper and lower sides prepared so that it might cover except the part connected to said connection member among the outside surfaces of said electrical and electric equipment/electronic parts laid underground and might stick to the plate thickness direction upper and lower sides of said electrical and electric equipment/electronic parts
The patchboard with built-in components characterized by providing.
[Claim 9]
They are two or more connectable direction conductive layers of a plate electrically to said conductive layer laid underground,
The interlayer connection object by the conductive bump who does the interlayer connection of said two or more direction conductive layers of a plate
The patchboard according to claim 8 with built-in components characterized by providing in a pan.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[Field of the Invention]

[0001]

This invention relates to the manufacture approach of a patchboard with built-in components, and a patchboard with built-in components, and relates to the manufacture approach of a patchboard with built-in components and the patchboard with built-in components which fit the further improvement in a component-mounting consistency especially.

[Background of the Invention]

[0002]

In recent years, an electronics technique progresses, and electronic equipment and communication equipment have advanced features, and the miniaturization is also progressing. In such a situation, by mounting to a patchboard, for example, a semi-conductor, in order to improve packaging density, the bare chip mounting method by package mounting has been put in practical use. Moreover, in passive components, such as a capacitor and resistance, the thing of a chip mounting mold is miniaturized to 0.6mmx0.3mm (0603) size.

[0003]

As the patchboard itself, the electrical installation between wiring layers (interlayer connection) has shifted to what forms a hole for each class by the CO2 laser or UV-YAG laser, and forms plating in the inside from what is depended on the conductive layer formed in the internal surface of a through hole, the thing filled up with a conductive paste (the so-called blind via). Moreover, the approach (additive method of construction) of replacing with the approach (subtractive method of construction) by etching, and carrying out metallizing formation of the wiring with plating is also being used for circuit pattern formation for the detailed-izing. Thereby, detailed formation is possible to

last shipment(Rhine/tooth space) =20micrometer / about 20 micrometers.

[0004]

In order to improve a component-mounting consistency further in such a situation and to ** to the miniaturization of a device, the patchboard with built-in components which contains components in a patchboard can be used. There are some which were indicated by JP,5-53269,U in a patchboard with built-in components.

[Patent reference 1] JP,5-53269,U

[Description of the Invention]

[Problem(s) to be Solved by the Invention]

[0005]

In what was indicated by the above-mentioned official report, the components mounted by building in a substrate are connected like the case where it is mounted on a substrate, on the land (naturally the plate thickness direction is formed perpendicularly) prepared corresponding to each terminal of components. Here, when components are built in in a substrate, as for the circumference of each [of the component], it is desirable to be covered and stuck by insulating resin except for the electrical installation section. It is because dependability will be degraded if a non-filling part is generated. At this point, when a clearance produces the thing of the above-mentioned official report between the substrates with which a component and this component are directly mounted on structure, being un-filled [of resin] up tends to produce this clearance very narrowly.

[0006]

This invention was made in consideration of the above-mentioned situation, and it aims at offering the manufacture approach of the patchboard with built-in components which can be improved in the further component-mounting consistency, and a patchboard with built-in components in the manufacture approach of a patchboard with built-in components, and a patchboard with built-in components, without spoiling dependability.

[Means for Solving the Problem]

[0007]

In order to solve the above-mentioned technical problem, the manufacture approach of the patchboard with built-in components concerning this invention The process which manufactures the core patchboard which has a conductive layer to vertical both sides at least, The process which forms the through tube to which a cross-section appearance becomes said manufactured core patchboard from two or more radii so that the space in which the electrical and electric equipment/electronic parts which should be built in should be located may be generated, The process which forms a conductive layer so that the internal surface of said formed through tube may be included, The process divided according to the number of the terminals of the electrical and electric equipment/electronic parts which should contain the process which carries out patterning of the conductive layer of said vertical both sides, and said conductive layer formed in said through tube, The process which connects the process which locates the electrical and electric equipment/electronic parts in said space, and said terminal and said divided conductive layer of said located electrical and electric equipment/electronic parts by the conductive member, It is characterized by providing the process which carries out laminating formation of the insulating layer so that it may put on each of vertical both sides of said core patchboard to which said electrical and electric equipment/electronic parts were connected by said conductive member and may be filled up with the surroundings of said electrical and electric equipment/electronic parts.

[0008]

It forms in the internal surface of the through tube which is the space in which the electrical and electric equipment/electronic parts which should contain the conductive layer for connecting with the terminal of built-in components are located by this manufacture approach. The formed conductive layer is divided according to the number of the terminals of built-in components. Therefore, make connection between the terminal of the component, and a conductive layer by the conductive member of the configuration which carried out the bridge horizontally.

Therefore, it becomes the structure which made the gap hard to produce around built-in components, and may be filled up and stuck to the insulating layer for a laminating around built-in components. Therefore, the patchboard which an opening does not occur [patchboard] and does not degrade dependability around built-in components can be manufactured.

[0009]

Moreover, the conductive layer which the cross-section configuration which the patchboard with built-in components concerning this invention was laid under the plate vertical side, without expressing, and was formed in the plate thickness direction becomes from two or more radii, The electrical and electric equipment/electronic parts laid underground in the plate so that it might have a terminal and said terminal might counter said conductive layer laid underground, The connection member which connects said terminal and said conductive layer electrically and mechanically, without being prepared in the gap of said terminal and said conductive layer of said electrical and electric equipment/electronic parts laid underground, and contacting the longitudinal direction edge of said conductive layer, It is characterized by providing the insulating layer of two upper and lower sides prepared so that it might cover except the part connected to said connection member among the outside surfaces of said electrical and electric equipment/electronic parts laid underground and might stick to the plate thickness direction upper and lower sides of said electrical and electric equipment/electronic parts.

[0010]

In this patchboard with built-in components, since the conductive layer for connecting with the terminal of built-in components is formed in the plate thickness direction and the cross-section configuration consists of two or more radii, the longitudinal direction width of face of a conductive layer has allowances of enough in connection with the built-in components through a connection member. Therefore, the connection between the terminal of the component and a conductive layer is made by the conductive member of the configuration which

carried out the bridge horizontally. Therefore, it becomes the structure which made the gap hard to produce, and the insulating layer of two upper and lower sides sticks to the surroundings of built-in components around built-in components. Therefore, an opening does not occur and dependability is not degraded around built-in components.

[Effect of the Invention]

[0011]

According to this invention, the conductive layer for connecting with the terminal of built-in components is formed in the plate thickness direction, therefore the connection between the terminal of the component and a conductive layer is made by the conductive member of the configuration which carried out the bridge horizontally. Therefore, it becomes the structure which made the gap hard to produce, and the insulating layer of two upper and lower sides may stick to the surroundings of built-in components around built-in components. Therefore, an opening does not occur and dependability is not degraded around built-in components.

[Best Mode of Carrying Out the Invention]

[0012]

Said process which forms a conductive layer as an embodiment of this invention so that the internal surface of said formed through tube may be included has the process which forms the conductive layer which serves as a substrate with nonelectrolytic plating, and the process which forms the conductive layer which uses said formed substrate for a seed and turns into the upper layer with electrolysis plating, and is made. Efficient plating formation can be performed by using two steps of such plating.

[0013]

Moreover, said process which forms the through tube to which a cross-section appearance becomes said manufactured core patchboard from two or more radii so that the space in which the electrical and electric equipment/electronic parts which should be built in should be located as an embodiment may be generated

can be made by drilling or metal mold punching. By using drilling, use of the existing manufacturing installations, such as a hole dawn machine for through holes, can be aimed at. Efficient through tube formation can be performed in metal mold punching.

[0014]

Moreover, as an embodiment, said process which locates the electrical and electric equipment/electronic parts in said space assigns supporter material to the bottom location of said core patchboard removed from said space, locates said electrical and electric equipment/electronic parts on said supporter material, and can be made. Although the mounting position of components is the space formed in the core patchboard, use of the existing manufacturing installations, such as the usual mounter, can be aimed at by using supporter material in this way.

[0015]

Moreover, as for said process which connects said terminal and said divided conductive layer of said located electrical and electric equipment/electronic parts by the conductive member, solder or conductive resin may be used as said conductive member as an embodiment. It is typical as available electric and mechanical-connections member.

[0016]

Moreover, the process divided according to the number of the terminals of the electrical and electric equipment/electronic parts which should contain as an embodiment said conductive layer formed in said through tube is made by drilling, metal mold punching, or laser beam machining.

[0017]

Moreover, said process which manufactures as an embodiment the core patchboard which has a conductive layer to vertical both sides at least manufactures the core patchboard which has four wiring layers, and it may be manufactured so that the electrical installation of these wiring layers may be made by the conductive bump. By setting a wiring layer to four, it considers as

the dimension from which space with built-in components tends to secure the thickness of a core patchboard, and much more high density assembly is realized by performing the interlayer connection of wiring layers by the conductive bump.

[0018]

Moreover, you may make it provide further the interlayer connection object by the conductive bump who does the interlayer connection of two or more connectable direction conductive layers of a plate, and said two or more direction conductive layers of a plate to said conductive layer laid underground electrically as an embodiment of a patchboard with built-in components.

[0019]

Below based on the above, the operation gestalt of this invention is explained, referring to a drawing. the sectional view (drawing 1 (a)) showing the typical configuration of the patchboard with built-in components which drawing 1 requires for 1 operation gestalt of this invention -- and it is a top view (drawing 1 (b)) a part.

[0020]

This operation gestalt is a four-layer patchboard which has insulating layers 11-14 and has wiring layers 21-24, respectively near the boundary of insulating layers 11 and 12, near the boundary of insulating layers 13 and 14, and in a vertical side, as shown in drawing 1 (a). The electrical installation between a wiring layer 21 and 22 and between a wiring layer 23 and 24 (interlayer connection) is made by the conductive bumps 41 and 42, respectively. The use effectiveness of a patchboard principal plane improves and it is suitable for high density assembly with such conductive bumps 41 and 42. Although the inside wiring layer 22 and the interlayer connection between 23 are not illustrated other than what is depended on the conductive layers 34 and 35 of a lengthwise direction, it is also possible to carry out by the so-called formation of a blind via etc. In addition, the signs 31 and 32 of a vertical side are solder resists.

[0021]

Moreover, the electrical and electric equipment / electronic parts 33 (for example, here chip resistor) is built in so that it may be contained in the level level of the inside wiring layers 22 and 23. The both-ends child faces the conductive layers 34 and 35 formed in the plate thickness direction through the solder 36 and 37 as a connection member, and components 33 are connected electrically and mechanically. Direct electrical installation with the inside wiring layers 22 and 23 is possible for conductive layers 34 and 35 so that it may illustrate.

[0022]

If it sees superficially, components 33 are arranged as shown in drawing 1 (b). That is, since components 33 are built in, the penetration space where a cross-section appearance consists of two or more radii is formed in the inside insulating layers 12 and 13, and this penetration space is occupied by components 33, the solder 36 and 37 for connecting, and the flash section inside the insulating layers 11 and 14 of vertical both sides. Solder 36 and 37 is the longitudinal direction edge (there may be generating of = production process top weld flash.) of conductive layers 34 and 35. detailed -- the after-mentioned. ****** -- it has not reached. In addition, by drawing 1 , although components 33 have a dimension smaller than the width of face which the direction of the thickness shown in drawing 1 (a) usually shows to drawing 1 (b), in order to carry out emphasis expansion and to show the thickness direction of a patchboard, the direction of thickness is greatly displayed also about components 33.

[0023]

when the chip resistor of 0603 is used for a concrete dimension (thickness) as components 33, the total thickness of insulating layers 12 and 13 is set to 0.2mm - about 0.3mm -- as -- these insulating layers 12 and 13 -- each is 0.1mm thru/or about 0.15mm in thickness. When using the larger (thick) thing as components than this, the insulating layers 12 and 13 which have the thickness according to it can be used. Although the thing of a single layer may be used for insulating layers 12 and 13, they have obtained predetermined thickness by the laminating of two layers with this operation gestalt.

[0024]
In addition, each part ingredient can use the conductive resin which distributed detailed metal grains (silver, copper, gold, solder, etc.) in resin for the conductive bumps 41 and 42, such as copper, at the wiring layers 21-24, such as an epoxy resin, polyimide resin, and bismaleimide triazine resin, or conductive layers 34 and 35 at insulating layers 11-14, for example. Moreover, about solder 36 and 37, it can replace with this and conductive resin can be used.
[0025]
Since it sticks so that insulating layers 11 and 14 may cover the surroundings of the built-in components 33 in the patchboard of the structure of this operation gestalt, and generating of an opening is prevented, it is very desirable to the improvement in dependability. In addition, although the chip resistor was made into the example as the electrical and electric equipment / electronic parts 33 and the above description explained, the same application is possible what has the arrangement structure of terminals, such as a chip capacitor, a chip inductor, and chip diode, almost the same as a chip resistor.
[0026]
Next, the example of the process which manufactures the patchboard with built-in components of the above structures is explained with reference to drawing 2 thru/or drawing 6 . Drawing 2 thru/or drawing 6 are drawings showing typically the process which manufactures the patchboard with built-in components concerning 1 operation gestalt of this invention in a cross section (or a part flat surface). In these drawings, the same sign is given to the same considerable part. Moreover, the same sign is given also to the patchboard shown in drawing 1 , and the corresponding part.
[0027]
the sectional view showing the production process of a up to as drawing 2 forms the through tube for components built-in in a core patchboard (patchboard material containing the layer in which components should be built) -- or it is a top view a part. First, as shown in drawing 2 (a), the laminating of the electric

insulating plates 12 and 13 is carried out, and the double-sided copper-clad sheet with which copper foil (thickness is 18 micrometers) 22a and 23a was arranged in the vertical side is prepared. This becomes a core patchboard.

[0028]

If a core patchboard is prepared next, as shown in drawing 2 (b1) and (b2), the through tube 51 which an appearance (cross-section appearance) becomes from two or more radii will be formed in the required location of a core patchboard. A through tube 51 is for forming the conductive layer of the plate thickness direction used for connection with built-in components, and serves as space in which built-in components are located. Here, although a through tube 51 is formed, every direction uses and carries out hole dawn of the NC (numerical control) drill of the diameter of 0.5mm at each edge (four places) of the cross-joint form which is 0.3mm (thereby, with a gestalt here, the cross-section appearance of a through tube 51 consists of four radii so that it may illustrate.). if a hole is broken with a drill -- a hole -- inside is washed by high-pressure water washing and the DESUMIA processing using a predetermined drug solution. In addition, metal mold punching can also be used for formation of a through tube 51.

[0029]

Next, as shown in drawing 2 (c1) and (c2), the copper plating layer 52 is formed for example, by 20-micrometer thickness so that the internal surface of a through tube 51 may be included. The seed layer which formed the seed layer of a continuation side with nonelectrolytic plating like chemistry copper plating for example first, and was formed after it can be made from carrying out electrolysis plating processing for example, in a copper-sulfate plating bath as a species at formation of the plating layer 52. The plating layer 52 can be efficiently formed with two steps of such plating.

[0030]

In addition, although the process shown in drawing 2 was explained as formation of the through tube 51 for components built-in, it is also explanation as a formation process of the interlayer connection by the so-called blind via mostly.

That is, when the electrical installation between the wiring layers by copper foil 22a and 23a is required, an interlayer connection can be made, if a through tube 51 and the same hole (however, it is simple may be circular.) are formed and a plating layer is further formed in the internal surface.

[0031]

the sectional view where drawing 3 shows the remaining production process which forms the through tube for components built-in to a core patchboard -- or it is a top view a part.

[0032]

If the plating layer 52 is formed as shown in drawing 2 (c1) and (c2) next, patterning will be performed to double-sided copper foil 22a and 23a (and plating layer 52 located in both sides), and wiring layers 22 and 23 will be formed. This patterning is copper foil 22a and 23a (the plating layer 52 located in both sides is included.) first, for example. It is ** to the following and degree paragraph. After carrying out chemical polishing of the front face and improving adhesion with the dry film for resists, the laminating of the dry film for resists is carried out to copper foil 22a and 23a. And a dry film is exposed with the alignment exposure machine which has an ultrahigh pressure mercury lamp through a photo mask, and spray development is further carried out by the sodium carbonate. The resist by which patterning was carried out is formed on copper foil 22a and 23a by leaving the dry film of this development pattern on copper foil 22a and 23a.

[0033]

If a resist is formed on copper foil 22a and 23a, spray etching of the copper foil 22a and 23a of the location which escaped from this as a resist pattern using the drug solution which uses ferric chloride as the base as etchant on the mask will be carried out. Thereby, wiring layers 22 and 23 are formed from copper foil 22a and 23a. in order for the formed wiring layers 22 and 23 to improve adhesion with the insulating layer by which a laminating is carried out after this -- melanism -- reduction processing is performed (the phase of drawing 6 (a) mentioned later is sufficient as this.). The formed wiring layers 22 and 23 contain the land part to

the plating layer 52 formed in the internal surface of a through tube 51 (the width of face is 0.2mm), as shown in drawing 3 (a2).

[0034]

Next, as shown in drawing 3 (b1), the plating layer 52 of through tube 51 internal surface is divided, and a core patchboard is processed so that independent formation of the conductive layers 34 and 35 which are connections with built-in components may be carried out. the hole with which NC drill was used for the processing approach here -- it is based on dawn. That is, the hole (plating layer fragmentation through tube) 53 with a diameter of about 0.4-0.5mm is broken in the location concerning the appearance border line of a through tube 51 which faces each other. According to fragmentation of the plating layer 52 by such drill, fragmentation formation of the conductive layers 34 and 35 can be easily carried out using existing equipment.

[0035]

The diameter of the plating layer fragmentation through tube 53 is made into one half extent of the maximum width of the through tube 51 whole, and it is made for the longitudinal direction dimension of the conductive layers 34 and 35 by which independent formation is carried out to have allowances by this here to the width of face of the components by which built-in mounting is carried out. Also when weld flash 53A (what remained without the plating layer's 52 exfoliating and mainly excising it.) will occur on a boundary with conductive layers 34 and 35 by formation of a hole 53 as shown in drawing 3 (b2) if it does in this way, it can prevent that this weld flash 53A interferes in mounting of built-in components. Since especially the process that removes this is not needed even if weld flash 53A occurs if it puts in another way, productivity can be improved (drawing 4 (b3) also makes reference.). In addition, it turns out that it will be easier to generate weld flash 53A if degradation of the cutting edge of the drill which ends a hole 53 progresses.

[0036]

The core patchboard with which the space (space by the through tube 51) for

building in components was formed of the above can be obtained. In addition, fragmentation of the plating layer 52 is above possible for making, even if not based on drilling. For example, the approach using punching (punching) by metal mold, a cutting machine, or laser beam machining is mentioned.

[0037]

the sectional view showing a component-mounting process for drawing 4 to build components in a core patchboard -- or it is a top view a part. First, as shown in drawing 4 (a), the single-sided field of a core patchboard is assigned to the supporter material 61, and components 33 are located in a predetermined location (space for building) by mounting devices, such as a mounter, in this condition. Here, the field top of the supporter material 61 is more desirable when adhesive layer 61a is prepared. It is because the mounted components 33 are fixed to some extent by adhesive layer 61a and degree process can be presented by it.

[0038]

In addition, it replaces with the supporter material 61 which has such adhesive layer 61a, and you may make it stick heat-resistant adhesive tape (or heat-resistant pressure sensitive adhesive sheet) on one side of a core patchboard.

[0039]

Next, as shown in drawing 4 (b1) and (b2), the cream solder 36a and 37a (solder, for example, Sn-3.0Ag- 0.5 lead of Cu free thing) is applied to the predetermined location near the both-ends child of components 33. Screen-stencil or a dispenser can perform such spreading. Here, the screen-stencil by the screen version which has the pit of the diameter of 0.4mm was used. In addition, the cream solder 36a and 37a may be replaced with this, and a conductive paste may be used for it.

[0040]

In mounting of components 33, and spreading of the cream solder 36a and 37a, as shown in drawing 4 (b3), also when weld flash 53A has arisen at the longitudinal direction edge of the conductive layer 34 for components connection

(35), the interference to these processes does not arise. That is, it is because the longitudinal direction dimension of a conductive layer 34 (35) is greatly secured to components 33, the generating location of weld flash 53A is avoided and mounting of components 33 and spreading of the cream solder 36a and 37a are possible. The through tube 51 beforehand formed in this semantics in order to locate components 33 may be formed so that that cross-section appearance may consist of many radii further not only in four radii.

[0041]

Next, the process which forms the insulating layer and conductive layer which should be carried out a laminating in both sides of the core patchboard with which components were mounted is explained with reference to drawing 5 here. Drawing 5 is the sectional view showing the process which forms the patchboard material for carrying out a laminating on a core patchboard. Such an insulating layer and a conductive layer are beforehand formed as a patchboard material.

[0042]

First, as shown in drawing 5 (a), copper foil (thickness is 18 micrometers) 21a (24a) is prepared, and conductive bump 41a (42a) of a cone form is mostly formed in the required location (location according to the layout of a specific patchboard) on this copper foil 21a (24a). In this, a conductive paste can be printed and made on copper foil 21a (24a) using screen-stencil.

[0043]

That in which the 0.2mm through tube (pit) was drilled can be used for the screen version in this case. Thereby, a conductive bump about 0.15mm or more can be formed as for example, a bottom surface diameter. as a conductive paste, metal grains (silver, gold, copper, solder, etc.) are distributed, for example in paste-like resin like an epoxy resin, and, in addition, an volatile solvent is mixed [having made and] -- it can use. After being printed, it dries in oven and a conductive paste is stiffened.

[0044]

Next, the prepreg (thickness is 0.06mm) which should be made an insulating

layer 11 (14) at copper foil 21a (24a) is made to counter using a special-purpose machine, and the prepreg of a semi-hardening condition is made to penetrate conductive bump 41a (42a), as shown in drawing 5 (b). Prepreg infiltrates hardenability resin like an epoxy resin into reinforcing materials like a glass fiber. Moreover, before hardening, it is in a semi-hardening condition, and it has thermoplasticity (fluidity by heat), and thermosetting. It refers to by the after-mentioned by using the thing of the condition which shows in drawing 5 (b) as patchboard materials 1a or 1b.

[0045]

Drawing 6 is drawing showing the process which forms the patchboard with built-in components as a finished product using the core patchboard with which components were mounted in a cross section. If the cream solder 36a and 37a is applied on a core patchboard as shown in drawing 4 (b1) and (b2) next, a reflow of the cream solder 36a and 37a will be carried out at a reflow furnace. This will be in the condition that it is shown in drawing 6 (a), and the solder 36 and 37 as a connection member will establish electric and mechanical connections of conductive layers 34 and 35 and the terminal of components 33. In addition, when it replaces with the cream solder 36a and 37a and a conductive paste is used, dry this in oven, it is made to harden, and electric and mechanical connections are established.

[0046]

in order for the core patchboard 4 of components wearing obtained by the above to improve adhesion with the insulating layer by which a laminating is carried out after this about the wiring layers 22 and 23 of those both sides -- melanism -- reduction processing is performed (this may already be made in drawing 3 (a1) and the phase of (a2)).

[0047]

Next, as shown in drawing 6 (b), the laminating of the patchboard materials 1a and 1b is carried out to the both sides of the core patchboard 4, and these are unified. The prepreg which should be made insulating layers 11 and 14 at this

time is stiffened. As the patchboard materials 1a and 1b were shown in drawing 5 , they are obtained.

[0048]

For example, layup equipment performs alignment in this laminating and unification, and the core patchboard 4 and the patchboard materials 1a and 1b are arranged in piles, and this is set as predetermined temperature and a predetermined pressure profile using a vacuum laminating heat press machine. A head is crushed by this laminating and unification, and deforms the conductive bumps 41 and 42 plastically by it, and electrical installation with wiring layers 22 or 23 establishes them.

[0049]

Moreover, a wiring layer 22 sinks to an insulating-layer 11 side by the thermoplasticity (fluidity by heat) of prepreg which should serve as an insulating layer 11, is located, is depressed to an insulating-layer 14 side with the thermoplasticity (fluidity by heat) of prepreg which should serve as an insulating layer 14, and comes to be located. [a wiring layer's 23] Furthermore, an insulating layer is formed also around it in one with insulating layers 11 and 14 so that the built-in components 33 may be covered and stuck by the thermoplasticity (fluidity by heat) of prepreg which should serve as insulating layers 11 and 14. thereby, the stopgap process of the circumference of components 33 is unnecessary, and the simplification of a process realizes it -- both, generating of a gap (void) is prevented and dependability can be improved.

[0050]

In addition, the patchboard materials 1a and 1b which carry out a laminating outside may be replaced with the thing of the gestalt shown in drawing 5 (b), and there may be still more wiring layers (for example, if the double-sided copper-clad sheet after patterning is used instead of copper foil 21a shown in drawing 5 (a), the number of wiring layers will be set to two in the phase of drawing 5 (b).). Moreover, the patchboard materials 1a and 1b which carry out a laminating outside do not necessarily need to be accompanied by conductive bump 41a

(42a), as shown in drawing 5 (b). In this case, since there is no conductive bump 41a (42a), although a conductive bump cannot perform, the interlayer connection of copper foil 21a (24a) and a wiring layer 22 (23) can establish a through hole in the patchboard after a laminating, and can form the interlayer connection structure by this through hole.

[0051]

If the laminating and unification of the insulating layer which should be located outside are done with the core patchboard 4 next, as shown in drawing 6 (c), patterning will be performed to the copper foil 21a and 24a of both outsides, and wiring layers 21 and 24 will be formed. This patterning can be performed like drawing 3 (a1) and the formation process of the wiring layers 22 and 23 which referred to (a2). That is, it is a procedure of exposure through chemical polishing, the dry film laminating for resists, and a photo mask, development, and etching. In addition, the laminating and unification of an insulating layer and copper foil (build up) may be done by the still more nearly same point as this outside after the laminating of the above outside insulating layers 11 and 14, a wiring layer 21, and formation of 24.

[0052]

Next, as shown in drawing 6 (c), the solder resists 31 and 32 are formed in the position of an outermost side. Furthermore, the layer (not shown) of nickel/gold (nickel is a substrate) is formed in the part in which the solder resist of wiring layers 21 or 24 is not formed by the nonelectrolytic plating method for corrosion prevention. And a patchboard is cut down so that it may become a predetermined appearance with a router processing machine. The patchboard with built-in components applied to this operation gestalt by the above can be obtained.

[0053]

With this operation gestalt, the existing thing can be used almost as it is as a manufacturing facility, and it leads to control of the manufacturing cost of a patchboard. Moreover, since the conductive bumps 41 and 42 were used for the

wiring layer 21 besides **, and the interlayer connection under 24, a wire length is shortened, it improves and a layout can do electrical characteristics as a patchboard efficiently. Moreover, since the chip resistor and chip capacitor with which mounting mark increase comparatively can be built in, relaxation and much more high density assembly of the present design Ruhr are possible. Furthermore, at the process for mounting and building in components 33, the good manufacture of the yield with very small defect generating by components mounting is possible. In addition, it sticks so that insulating layers 11 and 14 may cover the surroundings of the built-in components 33, and since generating of an opening is prevented, improvement in dependability is made.

[0054]

Next, the patchboard with built-in components concerning another operation gestalt of this invention is explained with reference to drawing 7 . Drawing 7 is the sectional view showing the typical configuration of the patchboard with built-in components concerning another operation gestalt of this invention. In drawing 7 , the same agreement is given to the same part as what was already explained in drawing 1 thru/or drawing 6 . Duplication is avoided and explained below.

[0055]

With this operation gestalt, it replaces with the insulating layers 12 and 13 of an inside laminating, and wiring layers 25 and 26 are formed near [those] the boundary using insulating layers 15, 16, and 17. Moreover, the conductive bumps 43, 44, and 45 are used for the interlayer connection between those adjoining wiring layers at least four layers of wiring layers 22 and 23 and wiring layers 25 and 26. Electrical installation with the inside direct wiring layers 25 and 26 is possible for the conductive layers 34 and 35 to which components 33 are connected through solder 36 and 37. In addition, the conductive bumps 43, 44, and 45 can form using screen-stencil which was explained by drawing 5 as the production process.

[0056]

The advantage of this operation gestalt is having made all the interlayer

connections by the conductive bump by performing an interlayer connection by three conductive bumps 43, 44, and 45 to the total thickness (total thickness [of insulating layers 15, 16, and 17]:, for example, 0.2mm) of the core patchboard for building in components 33. Here, by three conductive bumps 43, 44, and 45, bump formation high when there are few numbers than this is needed, and the interlayer connection of the core patchboard was carried out because an efficient conductive bump's formation was difficult. Thus, in required formation height, the difficulty like ** is not produced to about three, then the total thickness of about 0.2mm. Consequently, a core patchboard serves as a wiring layer of four layers, and serves as a wiring layer of six layers as a whole.

[0057]

However, if the conductive bumps' 43, 44, and 45 formation height is made higher, though the same components 33 are built in possible [making thicker prepreg penetrate] consequently, the number of the wiring layers of a core patchboard can be lessened. On the contrary, if the conductive bumps' 43, 44, and 45 formation height is made lower, thinner prepreg will be used and, as a result, the number of the wiring layers of a core patchboard can be made [many].

[0058]

What is necessary is to replace with the double-sided copper-clad sheet shown in drawing 2 (a), and just to use 4 lamellaes which use electric insulating plates 15, 16, and 17, copper foil 22a and 23a, wiring layers 25 and 26, and the conductive bumps 43, 44, and 45 as a component, in order to manufacture the patchboard with built-in components shown in drawing 7 . The subsequent process is the same as that of the thing and the essential target which showed drawing 6 from drawing 2 . What is necessary is just to repeat the process of a laminating for copper foil (or insulating layer with a wiring layer) to the side which counters in prepreg the conductive bump in whom it was printed and formed in and the conductive bump was formed after penetration (refer to drawing 5 for the above.), and penetration, in order to obtain 4 lamellaes.

[0059]
With this operation gestalt, the existing thing can be used almost as it is as a manufacturing facility like a previous operation gestalt, and it leads to control of the manufacturing cost of a patchboard. Moreover, at the process for mounting and building in components 33, the same is said of the good manufacture of the yield with very small defect generating by components mounting being possible. Furthermore, it is possible by setting the wiring layer in a core patchboard to four to realize much more high density assembly by considering as the dimension from which space with built-in components tends to secure the thickness of a core patchboard, and performing all of the interlayer connection of wiring layers by the conductive bumps 41-45.

[Brief Description of the Drawings]

[0060]

[Drawing 1] the sectional view showing the typical configuration of the patchboard with built-in components concerning 1 operation gestalt of this invention, and a part -- a top view.

[Drawing 2] Drawing showing typically the process which manufactures the patchboard with built-in components concerning 1 operation gestalt of this invention in a cross section (or a part flat surface).

[Drawing 3] Drawing showing typically the process which manufactures the patchboard with built-in components which is the ** Fig. of drawing 2 and is applied to 1 operation gestalt of this invention in a cross section (or a part flat surface).

[Drawing 4] Drawing showing typically the process which manufactures the patchboard with built-in components which is the ** Fig. of drawing 3 and is applied to 1 operation gestalt of this invention in a cross section (or a part flat surface).

[Drawing 5] Drawing showing typically the configuration of a patchboard material required for manufacture of the patchboard with built-in components concerning 1 operation gestalt of this invention in a cross section.

[Drawing 6] Drawing showing typically the process which manufactures the patchboard with built-in components which is the ** Fig. of drawing 4 and is applied to 1 operation gestalt of this invention in a cross section.
[Drawing 7] The sectional view showing the typical configuration of the patchboard with built-in components concerning another operation gestalt of this invention.
[Description of Notations]
[0061]
1a, 1b -- A patchboard material, 4 -- A patchboard material (core patchboard), 11, 12, 13, 14, 15, 16, 17 -- Insulating layer, 21, 22, 23, 24, 25, 26 -- A wiring layer, 21a, 22a, 23a, 24a -- 31 Copper foil, 32 -- A solder resist, 33 -- Electrical and electric equipment/electronic parts, 34 35 -- 36 A conductive layer, 37 -- Solder, 36a, 37a -- Cream solder, 41, 42, 43, 44, 45 [-- A plating layer 53 / -- A plating layer fragmentation through tube 53A / -- Weld flash 61 / -- Supporter material, 61a / -- Adhesive layer.] -- A conductive bump (after connection formation), 41a, 42a -- A conductive bump (before connection formation), 51 -- A through tube, 52

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[0060]

[Drawing 1] the sectional view showing the typical configuration of the patchboard with built-in components concerning 1 operation gestalt of this invention, and a part -- a top view.

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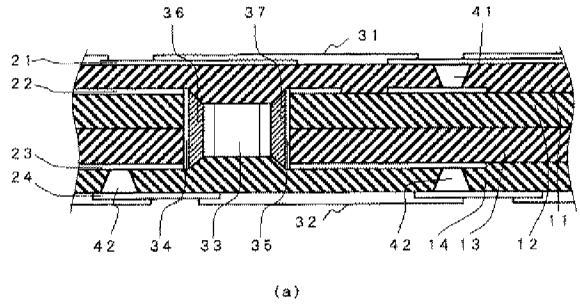
[Drawing 7] The sectional view showing the typical configuration of the patchboard with built-in components concerning another operation gestalt of this invention.

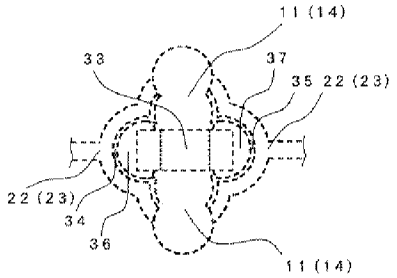
[Translation done.]

DRAWINGS

[Drawing 1]

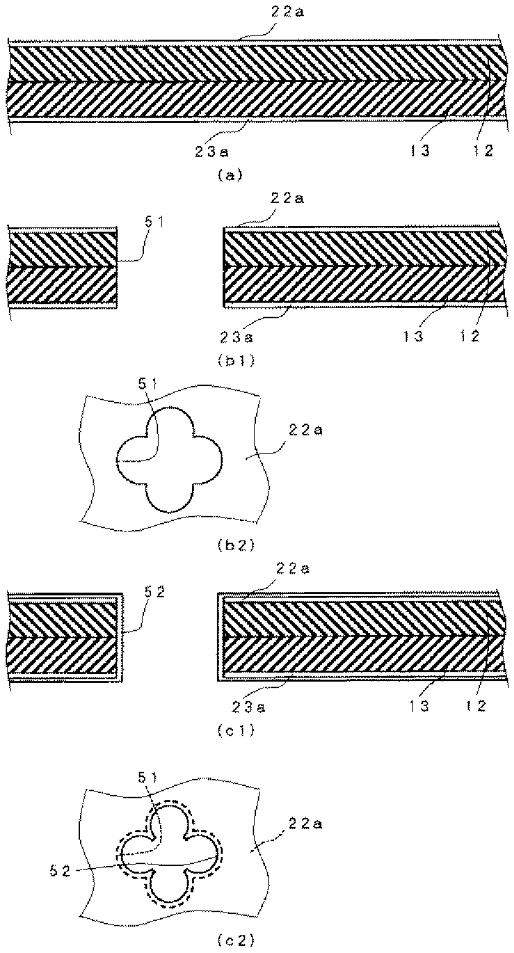


(a)



(b)

[Drawing 2]


22a
23a
13
12
(a)
51
22a
23a
13
12
(b1)
51
22a
(b2)
52
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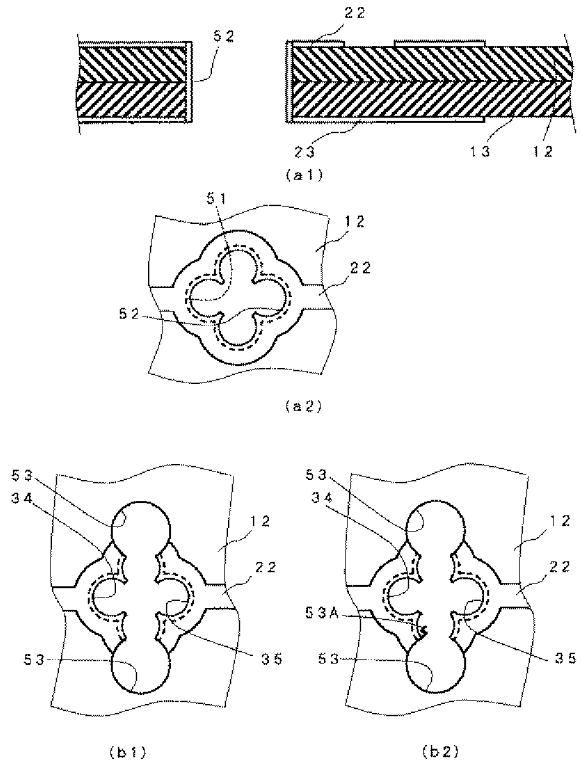
13
12
(c1)
51
22a
52
(c2)

[Drawing 3]


52
22
23
13
12
(a1)
51
12
22
52
(a2)
53
34
12
22
53
35
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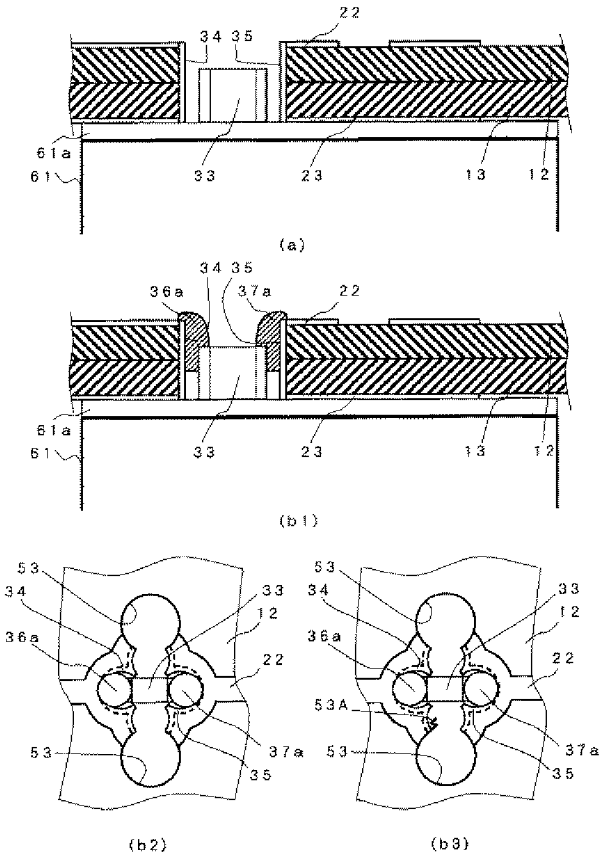
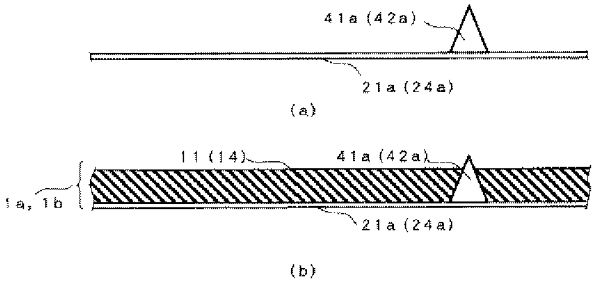
34
12
22
53A
53
35
(b2)

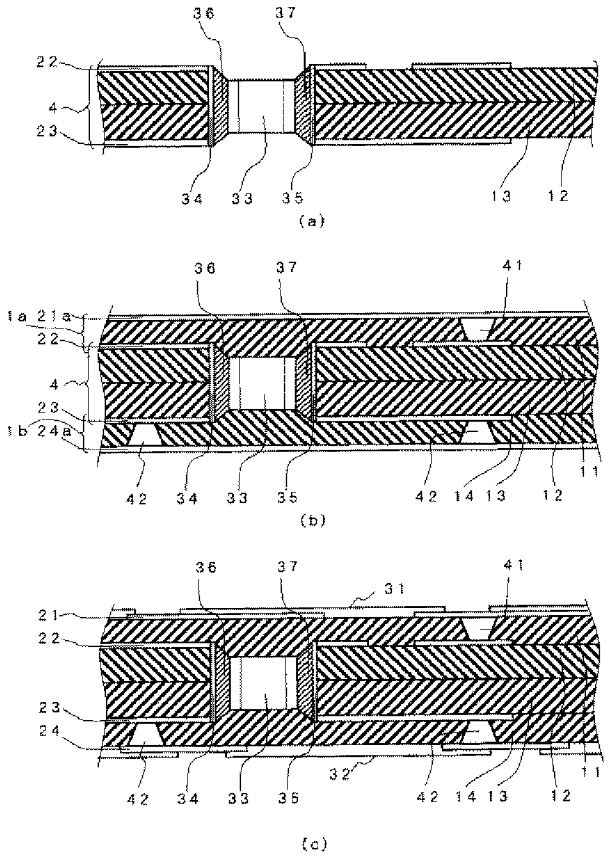
[Drawing 4]



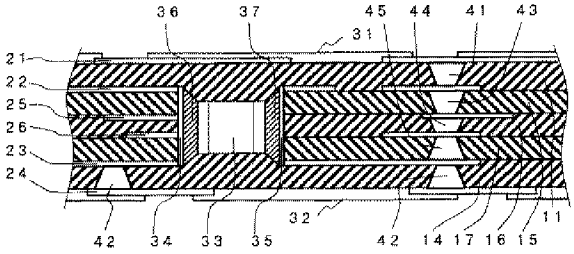
[Drawing 5]



[Drawing 6]



[Drawing 7]



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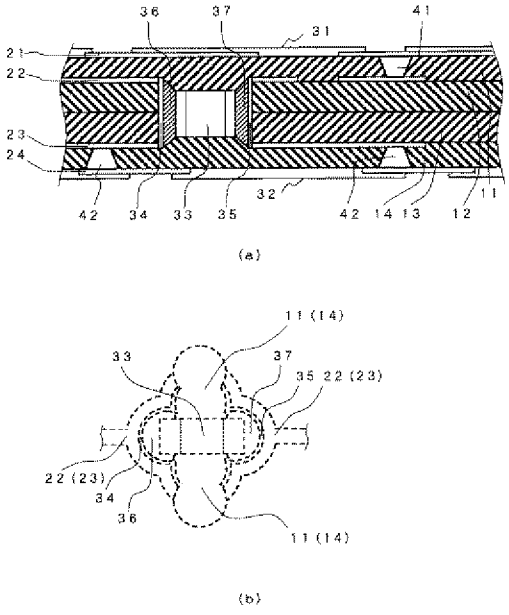
最終頁に続く

(54)【発明の名称】部品内蔵配線板の製造方法、部品内蔵配線板

(57)【要約】
【課題】部品内蔵配線板の製造方法および部品内蔵配線板において、信頼性を損なうことなくさらなる部品実装密度を向上する。
【解決手段】まず少なくとも上下両面に導電層を有するコア配線板を製造し、次に内蔵すべき電気／電子部品を位置させるべき空間が生じるように製造されたコア配線板に横断面外形が複数の円弧からなる貫通孔を形成し、次に形成された貫通孔の内表面を含むように導電層を形成し、次に上下両面の導電層をパターニングし、次に貫通孔に形成された導電層を内蔵すべき電気／電子部品の端子の数に応じて分断し、次に上記空間に電気／電子部品を位置させ、次に位置させられた電気／電子部品の端子と分断された導電層とを導電部材で接続し、次に導電部材により電気／電子部品が接続されたコア配線板の上下両面それぞれに重ねてかつ電気／電子部品の周りを充填するように絶縁層を積層形成する。
【選択図】図１



【特許請求の範囲】
【請求項1】
少なくとも上下両面に導電層を有するコア配線板を製造する工程と、
内蔵すべき電気／電子部品を位置させるべき空間が生じるように前記製造されたコア配線板に横断面外形が複数の円弧からなる貫通孔を形成する工程と、
前記形成された貫通孔の内表面を含むように導電層を形成する工程と、
前記上下両面の導電層をパターニングする工程と、
前記貫通孔に形成された前記導電層を内蔵すべき電気／電子部品の端子の数に応じて分断する工程と、
前記空間に電気／電子部品を位置させる工程と、
前記位置させられた電気／電子部品の前記端子と前記分断された導電層とを導電部材で接続する工程と、
前記導電部材により前記電気／電子部品が接続された前記コア配線板の上下両面それぞれに重ねてかつ前記電気／電子部品の周りを充填するように絶縁層を積層形成する工程と
を具備することを特徴とする部品内蔵配線板の製造方法。
【請求項2】
前記形成された貫通孔の内表面を含むように導電層を形成する前記工程が、無電解めっきにより下地となる導電層を形成する工程と、前記形成された下地を種に用いて電解めっきにより上層となる導電層を形成する工程とを有することを特徴とする請求項１記載の部品内蔵配線板の製造方法。
【請求項3】
内蔵すべき電気／電子部品を位置させるべき空間が生じるように前記製造されたコア配線板に横断面外形が複数の円弧からなる貫通孔を形成する前記工程が、ドリリング、または金型打ち抜きによりなされることを特徴とする請求項１記載の部品内蔵配線板の製造方法。
【請求項4】
前記空間に電気／電子部品を位置させる前記工程が、前記空間からのぞく前記コア配線板の下位置に支持部材をあてがい、前記支持部材上に前記電気／電子部品を位置させてなされることを特徴とする請求項１記載の部品内蔵配線板の製造方法。
【請求項5】
前記位置させられた電気／電子部品の前記端子と前記分断された導電層とを導電部材で接続する前記工程が、前記導電部材として半田または導電性樹脂が用いられることを特徴とする請求項１記載の部品内蔵配線板の製造方法。
【請求項6】
前記貫通孔に形成された前記導電層を内蔵すべき電気／電子部品の端子の数に応じて分断する工程が、ドリリング、金型打ち抜き、またはレーザ加工によりなされることを特徴とする請求項１記載の部品内蔵配線板の製造方法。
【請求項7】
少なくとも上下両面に導電層を有するコア配線板を製造する前記工程が、配線層を４つ有するコア配線板を製造するものであり、かつ、これらの配線層同士の電気的接続が導電性バンプでなされるように製造されることを特徴とする請求項１ないし６のいずれか１項記載の部品内蔵配線板の製造方法。
【請求項8】
板上下面には表出せずに埋設されて板厚み方向に形成された、横断面形状が複数の円弧からなる導電層と、
端子を有し、前記埋設された導電層に前記端子が対向するように板内埋設された電気／電子部品と、
前記埋設された電気／電子部品の前記端子と前記導電層との間隙に設けられ、前記導電層の横方向端部に接触せずに前記端子と前記導電層とを電気的・機械的に接続する接続部

材と、
　前記埋設された電気／電子部品の外表面のうち前記接続部材に接続される部位以外を覆いかつ前記電気／電子部品の板厚み方向上下に密着するように設けられた上下２つの絶縁層と
　を具備することを特徴とする部品内蔵配線板。
【請求項9】
　前記埋設された導電層に電気的に接続可能な複数の板方向導電層と、
　前記複数の板方向導電層を層間接続する導電性バンプによる層間接続体と
【発明の詳細な説明】とを特徴とする請求項８記載の部品内蔵配線板。
【技術分野】
【0001】
　本発明は、部品内蔵配線板の製造方法および部品内蔵配線板に係り、特に、さらなる部品実装密度向上に適する部品内蔵配線板の製造方法および部品内蔵配線板に関する。
【背景技術】
【0002】
　近年、エレクトロニクス技術が進展し電子機器や通信機器が高機能化され、かつ小型化も進んでいる。このような状況で配線板への例えば半導体の実装では、実装密度を向上するためパッケージ実装によらないベアチップ実装法が実用化されてきている。また、コンデンサや抵抗などの受動部品では、チップ実装型のものが、０．６ｍｍ×０．３ｍｍ（０６０３）のサイズまで小型化している。
【0003】
　配線板自体としては、配線層間の電気的接続（層間接続）が、スルーホールの内表面に形成された導電層によるものから、CO_2レーザやＵＶ－ＹＡＧレーザにより各層ごとにホールを形成しその内側にめっきを形成するものや導電性ペーストを充填するものなど（いわゆるブラインドビア）に移行している。また、配線パターン形成には、その微細化のため、エッチングによる方法（サブトラクティブ工法）に代えてめっきにより配線をメタライズ形成する方法（アディティブ工法）も使用されつつある。これにより、Ｌ／Ｓ（ライン／スペース）＝２０μｍ／２０μｍ程度まで微細形成可能となっている。
【0004】
　このような状況でさらに部品実装密度を向上し機器の小型化に資するには、例えば、配線板内に部品を内蔵する部品内蔵配線板を用いることができる。部品内蔵配線板には、例えば、実開平５－５３２６９号公報に開示されたものがある。
【特許文献1】実開平５－５３２６９号公報
【発明の開示】
【発明が解決しようとする課題】
【0005】
　上記公報に開示されたものでは、基板内に内蔵して実装される部品は、基板上に実装される場合と同様に、部品の端子それぞれに対応して設けられたランド（当然、板厚み方向とは垂直方向に形成されている）上に接続される。ここで、部品が基板内に内蔵される場合には、その部品の各周りは電気的接続部を除いて絶縁樹脂で覆われ密着されるのが好ましい。未充填部位が生じると信頼性を劣化させるからである。この点で、上記公報のものは、構造上、部品とこの部品が直接実装される基板との間に隙間が生じた場合、この隙間は非常に狭く樹脂の未充填が生じやすい。
【0006】
　本発明は、上記した事情を考慮してなされたもので、部品内蔵配線板の製造方法および部品内蔵配線板において、信頼性を損なうことなくさらなる部品実装密度を向上することが可能な部品内蔵配線板の製造方法および部品内蔵配線板を提供することを目的とする。
【課題を解決するための手段】
【0007】
　上記の課題を解決するため、本発明に係る部品内蔵配線板の製造方法は、少なくとも上

下両面に導電層を有するコア配線板を製造する工程と、内蔵すべき電気／電子部品を位置させるべき空間が生じるように前記製造されたコア配線板に横断面外形が複数の円弧からなる貫通孔を形成する工程と、前記形成された貫通孔の内表面を含むように導電層を形成する工程と、前記上下両面の導電層をパターニングする工程と、前記貫通孔に形成された前記導電層を内蔵すべき電気／電子部品の端子の数に応じて分断する工程と、前記空間に電気／電子部品を位置させる工程と、前記位置させられた電気／電子部品の前記端子と前記分断された導電層とを導電部材で接続する工程と、前記導電部材により前記電気／電子部品が接続された前記コア配線板の上下両面それぞれに重ねてかつ前記電気／電子部品の周りを充填するように絶縁層を積層形成する工程とを具備することを特徴とする。

【0008】

この製造方法では、内蔵部品の端子に接続するための導電層を、内蔵すべき電気／電子部品を位置させる空間である貫通孔の内表面に形成する。形成された導電層は内蔵部品の端子の数に応じて分断される。したがって、その部品の端子と導電層との接続は、例えば水平方向にブリッジした形状の導電部材によりなされ得る。よって、内蔵部品の周りに間隙を生じにくくした構造となり、内蔵部品の周りには積層のための絶縁層が充填・密着され得る。したがって、内蔵部品の周辺に空隙が発生せず信頼性を劣化させない配線板を製造することができる。

【0009】

また、本発明に係る部品内蔵配線板は、板上下面には表出せずに埋設されて板厚み方向に形成された、横断面形状が複数の円弧からなる導電層と、端子を有し、前記埋設された導電層に前記端子が対向するように板内埋設された電気／電子部品と、前記埋設された電気／電子部品の前記端子と前記導電層との間隙に設けられ、前記導電層の横方向端部に接触せずに前記端子と前記導電層とを電気的・機械的に接続する接続部材と、前記埋設された電気／電子部品の外表面のうち前記接続部材に接続される部位以外を覆いかつ前記電気／電子部品の板厚み方向上下に密着するように設けられた上下２つの絶縁層とを具備することを特徴とする。

【0010】

この部品内蔵配線板では、内蔵部品の端子に接続するための導電層が、板厚み方向に形成されておりかつ横断面形状が複数の円弧からなっているので導電層の横方向幅は接続部材を介する内蔵部品との接続に十分余裕がある。したがって、その部品の端子と導電層との接続は、例えば水平方向にブリッジした形状の導電部材によりなされる。よって、内蔵部品の周りに間隙を生じにくくした構造となり、内蔵部品の周りには上下２つの絶縁層が密着する。したがって、内蔵部品の周辺に空隙が発生せず信頼性を劣化させない。

【発明の効果】

【0011】

本発明によれば、内蔵部品の端子に接続するための導電層が板厚み方向に形成され、したがって、その部品の端子と導電層との接続は、例えば水平方向にブリッジした形状の導電部材によりなされる。よって、内蔵部品の周りに間隙を生じにくくした構造となり、内蔵部品の周りには上下２つの絶縁層が密着し得る。ゆえに、内蔵部品の周辺に空隙が発生せず信頼性を劣化させない。

【発明を実施するための最良の形態】

【0012】

本発明の実施態様として、前記形成された貫通孔の内表面を含むように導電層を形成する前記工程は、無電解めっきにより下地となる導電層を形成する工程と、前記形成された下地を種に用いて電解めっきにより上層となる導電層を形成する工程とを有してなされる。このような２段階のめっきを用いることで効率的なめっき形成を行なうことができる。

【0013】

また、実施態様として、内蔵すべき電気／電子部品を位置させるべき空間が生じるように前記製造されたコア配線板に横断面外形が複数の円弧からなる貫通孔を形成する前記工程は、ドリリングまたは金型打ち抜きによりなすことができる。ドリリングを用いること

で、スルーホール用の穴明け機など既存の製造装置の利用を図ることができる。金型打ち抜きでは効率的な貫通孔形成ができる

【0014】

また、実施態様として、前記空間に電気／電子部品を位置させる前記工程は、前記空間からのぞく前記コア配線板の下位置に支持部材をあてがい、前記支持部材上に前記電気／電子部品を位置させてなすことができる。部品の実装位置は、コア配線板に形成された空間であるが、このように支持部材を利用することで、通常のマウンタなど既存の製造装置の利用を図ることができる。

【0015】

また、実施態様として、前記位置させられた電気／電子部品の前記端子と前記分断された導電層とを導電部材で接続する前記工程は、前記導電部材として半田または導電性樹脂が用いられ得る。利用可能な電気的・機械的接続部材として代表的なものである。

【0016】

また、実施態様として、前記貫通孔に形成された前記導電層を内蔵すべき電気／電子部品の端子の数に応じて分断する工程は、ドリリング、金型打ち抜き、またはレーザ加工によりなされる。

【0017】

また、実施態様として、少なくとも上下両面に導電層を有するコア配線板を製造する前記工程は、配線層を４つ有するコア配線板を製造するものであり、かつ、これらの配線層同士の電気的接続が導電性バンプでなされるように製造され得る。配線層を４つとすることにより、コア配線板の厚さを部品内蔵空間が確保しやすい寸法とし、配線層同士の層間接続を導電性バンプで行なうことにより一層の高密度実装を実現する。

【0018】

また、部品内蔵配線板の実施態様として、前記埋設された導電層に電気的に接続可能な複数の板方向導電層と、前記複数の板方向導電層を層間接続する導電性バンプによる層間接続体とをさらに具備するようにしてもよい。

【0019】

以上を踏まえ、以下では本発明の実施形態を図面を参照しながら説明する。図１は、本発明の一実施形態に係る部品内蔵配線板の模式的な構成を示す断面図（図１（ａ））および一部平面図（図１（ｂ））である。

【0020】

この実施形態は、図１（ａ）に示すように、絶縁層１１～１４を有し、絶縁層１１、１２の境界付近、絶縁層１３、１４の境界付近、および上下面に配線層２１～２４をそれぞれ有する４層配線板である。配線層２１、２２間、および配線層２３、２４間の電気的接続（層間接続）は導電性バンプ４１、４２によりそれぞれなされている。このような導電性バンプ４１、４２により、配線板主面の利用効率が向上し高密度実装に適する。内側の配線層２２、２３間の層間接続は、縦方向の導電層３４、３５によるもの以外は図示していないが、いわゆるブラインドビアなどの形成により行うことも可能である。なお、上下面の符号３１、３２は、半田レジストである。

【0021】

また、内側の配線層２２、２３の水平レベル内に含まれるように電気／電子部品３３（例えばここではチップ抵抗）が内蔵される。部品３３は、その両端子が接続部材としての半田３６、３７を介して、板厚み方向に形成された導電層３４、３５に向かい合いかつ電気的、機械的に接続されている。導電層３４、３５は、図示するように、内側の配線層２２、２３との直接的な電気的接続が可能となっている。

【0022】

部品３３は、平面的に見ると図１（ｂ）に示すように配設されている。すなわち、部品３３を内蔵するため内側の絶縁層１２、１３には、横断面外形が複数の円弧からなる貫通空間が形成され、この貫通空間は、部品３３および接続するための半田３６、３７ならびに上下両側の絶縁層１１、１４の内側へのはみ出し部により占められている。半田３６、

３７は、導電層３４、３５の横方向端部（＝製造工程上バリの発生があり得る。詳しくは後述。）までは達していない。なお、部品３３は、通常、図１（ａ）に示す厚さの方が図１（ｂ）に示す幅より寸法が小さいが、図１では配線板の厚み方向を強調拡大して示すため部品３３についても厚さの方が大きく表示されている。

【0023】

具体的な寸法（厚さ）は、部品３３として０６０３のチップ抵抗を使用したとき、絶縁層１２、１３の合計厚が例えば０．２ｍｍ～０．３ｍｍ程度となるように、これらの絶縁層１２、１３それぞれが０．１ｍｍないし０．１５ｍｍ程度の厚さである。部品としてこれより大きい（厚い）ものを用いる場合には、それに応じた厚さを有する絶縁層１２、１３を用いることができる。絶縁層１２、１３は、単一の層のものを用いてもよいが、この実施形態では２つの層の積層により所定の厚さを得ている。

【0024】

なお、各部材料は、絶縁層１１～１４には例えばエポキシ樹脂、ポリイミド樹脂、ビスマレイミドトリアジン樹脂など、配線層２１～２４や導電層３４、３５には例えば銅など、導電性バンプ４１、４２には、例えば微細な金属粒（銀、銅、金、半田など）を樹脂中に分散させた導電性樹脂などを用いることができる。また、半田３６、３７については、これに代えて導電性樹脂を用いることができる。

【0025】

この実施形態の構造の配線板では、内蔵された部品３３の周りを絶縁層１１、１４が覆うように密着し、空隙の発生を防止するので信頼性向上に極めて好ましい。なお、以上の記述では、電気／電子部品３３としてチップ抵抗を例にして説明したが、チップコンデンサ、チップインダクタ、チップダイオードなど端子の配置構造がチップ抵抗とほぼ同じものでは同様な適用が可能である。

【0026】

次に、上記のような構造の部品内蔵配線板を製造するプロセスの例を図２ないし図６を参照して説明する。図２ないし図６は、本発明の一実施形態に係る部品内蔵配線板を製造するプロセスを模式的に断面（または一部平面）にて示す図である。これらの図において、同一相当の部位には同一符号を付してある。また、図１に示す配線板と対応する部位にも同一符号を付してある。

【0027】

図２は、コア配線板（部品が内蔵されるべき層を含む配線板素材）に部品内蔵用の貫通孔を形成する途中までの製造工程を示す断面図または一部平面図である。まず、図２（ａ）に示すように、絶縁板１２、１３が積層され、その上下面に銅箔（厚さは例えば１８μｍ）２２ａ、２３ａが配設された両面銅張り板を用意する。これがコア配線板になる。

【0028】

コア配線板が用意されたら、次に、図２（ｂ１）、（ｂ２）に示すように、コア配線板の必要な位置に、外形（横断面外形）が複数の円弧からなる貫通孔５１を形成する。貫通孔５１は、内蔵部品との接続に用いる、板厚み方向の導電層を形成するためのものであり、かつ内蔵部品を位置させる空間となるものである。ここでは、貫通孔５１を形成するのに、縦横とも０．３ｍｍである十字形の各端部（４箇所）に０．５ｍｍ径のＮＣ（numerical control）ドリルを用いて穴明けする（これにより、ここでの形態では貫通孔５１の横断面外形は図示するように４つの円弧からなる。）。ドリルにより孔を明けたら、孔内を、例えば高圧水洗浄および所定の薬液を用いるデスミア処理で洗浄しておく。なお、貫通孔５１の形成に金型打ち抜きを用いることもできる。

【0029】

次に、図２（ｃ１）、（ｃ２）に示すように、貫通孔５１の内壁面を含むように例えば銅のめっき層５２を例えば２０μｍ厚で形成する。めっき層５２の形成には、例えば、まず、化学銅めっきのような無電解めっきにより連続面のシード層を形成し、そのあと、形成されたシード層を種に例えば硫酸銅めっき浴にて電解めっき処理することよりなすことができる。このような２段階のめっきにより効率的にめっき層５２を形成することができ

る。

【0030】

なお、図２に示す工程は、部品内蔵用の貫通孔５１の形成として説明したが、いわゆるブラインドビアによる層間接続の形成工程としての説明にもほぼなっている。すなわち、銅箔２２ａ、２３ａによる配線層の間の電気的接続が必要な場合には、貫通孔５１と同様な孔（ただし単純な円形でよい。）を形成し、さらにその内壁面にめっき層を形成すれば層間接続を形設することができる。

【0031】

図３は、コア配線板に部品内蔵用の貫通孔を形成する残りの製造工程を示す断面図または一部平面図である。

【0032】

図２（ｃ１）、（ｃ２）に示すようにめっき層５２が形成されたら、次に、両面の銅箔２２ａ、２３ａ（、および両面に位置するめっき層５２）にパターニングを施し配線層２２、２３を形成する。このパターニングは、例えば、まず、銅箔２２ａ、２３ａ（両面に位置するめっき層５２を含む。以下、次段落まで同。）の表面を化学研磨してレジスト用のドライフィルムとの密着性を向上したうえで、レジスト用ドライフィルムを銅箔２２ａ、２３ａに積層する。そして、フォトマスクを介して例えば超高圧水銀灯を有するアライメント露光機でドライフィルムを露光し、さらに炭酸ナトリウムによってスプレー現像する。この現像パターンのドライフィルムを銅箔２２ａ、２３ａ上に残すことにより、パターニングされたレジストが銅箔２２ａ、２３ａ上に形成される。

【0033】

レジストが銅箔２２ａ、２３ａ上に形成されたら、これをマスクにエッチャントとして塩化第２鉄をベースとする薬液を用い、レジストパターンとして抜けた位置の銅箔２２ａ、２３ａをスプレーエッチングする。これにより、銅箔２２ａ、２３ａから配線層２２、２３が形成される。形成された配線層２２、２３は、このあと積層される絶縁層との密着性を向上するために黒化還元処理を行なっておく（これは、後述する図６（ａ）の段階でもよい。）。形成された配線層２２、２３は、図３（ａ２）に示すように、貫通孔５１の内壁面に形成されためっき層５２に対してのランド部分（その幅は例えば０．２ｍｍ）を含む。

【0034】

次に、図３（ｂ１）に示すように、貫通孔５１内壁面のめっき層５２を分断して内蔵部品との接続部である導電層３４、３５を独立形成するようにコア配線板を加工する。ここでの加工方法は、ＮＣドリルを用いた孔明けによる。すなわち、貫通孔５１の外形輪郭線にかかる向い合う位置に例えば直径０．４～０．５ｍｍ程度の孔（めっき層分断貫通孔）５３を明ける。このようなドリルによるめっき層５２の分断によれば、既存の装置を用いて容易に導電層３４、３５を分断形成することができる。

【0035】

ここで、めっき層分断貫通孔５３の直径は貫通孔５１全体の最大幅の半分程度とし、これにより、独立形成される導電層３４、３５の横方向寸法が内蔵実装される部品の幅に対して余裕を有するようにする。このようにすると、図３（ｂ２）に示すように孔５３の形成によってバリ５３Ａ（主にめっき層５２が剥離して切除されずに残ったもの。）が導電層３４、３５との境界に発生する場合にも、このバリ５３Ａが内蔵部品の実装に干渉することを防止できる。換言すると、バリ５３Ａが発生してもこれを取り除く工程を特に必要としないので生産性を向上できる（図４（ｂ３）でも言及する。）。なお、バリ５３Ａは、孔５３を明けるドリルの刃の劣化が進むとより発生しやすいことが分かっている。

【0036】

以上により、部品を内蔵するための空間（貫通孔５１による空間）が形成されたコア配線板を得ることができる。なお、上記でめっき層５２の分断は、ドリリングによらなくてもなすことは可能である。例えば金型による打ち抜き（パンチング）や切削機、またはレーザ加工を用いる方法が挙げられる。

【0037】
図４は、コア配線板に部品を内蔵するための部品実装工程を示す断面図または一部平面図である。まず、図４（ａ）に示すように、コア配線板の片側面を支持部材６１にあてがい、この状態において、マウンタなどの実装機器により所定位置（内蔵するための空間）に部品３３を位置させる。ここで、支持部材６１の面上は、粘着層６１ａを設けるようにするとより好ましい。粘着層６１ａにより、マウントされた部品３３がある程度固定されて次工程に供することができるからである。
【0038】
なお、このような粘着層６１ａを有する支持部材６１に代えて、耐熱性の粘着テープ（または耐熱性の粘着シート）をコア配線板の片面に張り付けるようにしてもよい。
【0039】
次に、図４（ｂ１）、（ｂ２）に示すように、部品３３の両端子付近の所定位置にクリーム半田３６ａ、３７ａ（半田は、例えばＳｎ－３．０Ａｇ－０．５Ｃｕの鉛フリーのもの）を塗布する。このような塗布は、例えばスクリーン印刷またはディスペンサにより行なうことができる。ここでは、０．４ｍｍ径のピットを有するスクリーン版によるスクリーン印刷を用いた。なお、クリーム半田３６ａ、３７ａは、これに代えて導電性ペーストを用いてもよい。
【0040】
部品３３のマウント、およびクリーム半田３６ａ、３７ａの塗布においては、図４（ｂ３）に示すように、部品接続用の導電層３４（３５）の横方向端部にバリ５３Ａが生じている場合にも、これらの工程への干渉が生じない。すなわち、導電層３４（３５）の横方向寸法が部品３３に対して大きく確保されており、バリ５３Ａの発生位置を避けて部品３３のマウント、およびクリーム半田３６ａ、３７ａの塗布が可能だからである。この意味で、部品３３を位置させるためあらかじめ形成する貫通孔５１は、その横断面外形が４つの円弧に限らずさらに多数の円弧からなるように形成されていてもよい。
【0041】
次に、ここで、部品の実装されたコア配線板の両面に積層すべき絶縁層および導電層を形成する工程について図５を参照して説明する。図５は、コア配線板上に積層するための配線板素材を形成する工程を示す断面図である。このような絶縁層および導電層はあらかじめ配線板素材として形成しておく。
【0042】
まず、図５（ａ）に示すように、銅箔（厚さは例えば１８μｍ）２１ａ（２４ａ）を用意し、この銅箔２１ａ（２４ａ）上の必要な位置（特定の配線板のレイアウトに従う位置）にほぼ円錐形の導電性バンプ４１ａ（４２ａ）を形成する。これには、例えばスクリーン印刷を用いて導電性ペーストを銅箔２１ａ（２４ａ）上に印刷してなすことができる。
【0043】
この場合のスクリーン版には、例えば０．２ｍｍの貫通孔（ピット）が穿設されたものを用いることができる。これにより、例えば底面径として０．１５ｍｍ程度以上の導電性バンプを形成することができる。導電性ペーストとしては、例えばエポキシ樹脂のようなペースト状樹脂の中に金属粒（銀、金、銅、半田など）を分散させ、加えて揮発性の溶剤を混合させたもの用いることができる。印刷されたあと、例えばオーブンで乾燥し導電性ペーストを硬化させる。
【0044】
次に、専用機を用い、銅箔２１ａ（２４ａ）に絶縁層１１（１４）とすべきプリプレグ（厚さは例えば０．０６ｍｍ）に対向させて、図５（ｂ）に示すように、導電性バンプ４１ａ（４２ａ）を半硬化状態のプリプレグに貫通させる。プリプレグは、例えば、エポキシ樹脂のような硬化性樹脂をガラス繊維のような補強材に含浸させたものである。また、硬化する前には半硬化状態にあり、熱可塑性（熱による流動性）および熱硬化性を有する。図５（ｂ）に示す状態のものを配線板素材１ａまたは１ｂとして後述で参照する。
【0045】

図６は、部品の実装されたコア配線板を用いて完成品としての部品内蔵配線板を形成する工程を断面で示す図である。図４（ｂ１）、（ｂ２）に示すようにクリーム半田３６ａ、３７ａをコア配線板上に塗布したら、次に、クリーム半田３６ａ、３７ａをリフロー炉でリフローさせる。これにより、図６（ａ）に示すような状態となり、接続部材としての半田３６、３７が導電層３４、３５と部品３３の端子との電気的・機械的接続を確立する。なお、クリーム半田３６ａ、３７ａに代えて導電性ペーストを用いた場合には、これを例えばオーブンで乾燥させ硬化させて電気的・機械的接続を確立する。

【0046】

以上により得られた部品装着のコア配線板４は、その両面の配線層２２、２３についてこのあと積層される絶縁層との密着性を向上するため黒化還元処理を行なっておく（これは、すでに図３（ａ１）、（ａ２）の段階でなされている場合もある。）。

【0047】

次に、図６（ｂ）に示すように、コア配線板４の両側に配線板素材１ａ、１ｂを積層し、これらを一体化する。このとき絶縁層１１、１４とすべきプリプレグを硬化させる。配線板素材１ａ、１ｂは、図５に示したようにして得られたものである。

【0048】

この積層・一体化には、例えばレイアップ装置で位置合わせを行いコア配線板４と配線板素材１ａ、１ｂとを重ねて配置し、かつ真空積層熱プレス機を用いこれを所定の温度および圧力プロファイルに設定する。この積層・一体化により導電性バンプ４１、４２は、頭部がつぶされて塑性変形し、配線層２２または２３との電気的接続が確立する。

【0049】

また、配線層２２は、絶縁層１１となるべきプリプレグの熱可塑性（熱による流動性）により絶縁層１１側へ沈み込んで位置し、配線層２３は、絶縁層１４となるべきプリプレグの熱可塑性（熱による流動性）により絶縁層１４側へ沈み込んで位置するようになる。さらに、絶縁層１１、１４となるべきプリプレグの熱可塑性（熱による流動性）により、内蔵された部品３３を覆いかつ密着するようにその周辺にも絶縁層が絶縁層１１、１４と一体的に形成される。これにより部品３３周りの穴埋め工程は不要であり工程の簡素化が実現するとともに、間隙（ボイド）の発生を防止して信頼性を向上できる。

【0050】

なお、外側に積層する配線板素材１ａ、１ｂは図５（ｂ）に示す形態のものに代えて、さらに配線層数が多いものでもよい（例えば、図５（ａ）に示す銅箔２１ａの代わりにパターニング後の両面銅張り板を用いれば、図５（ｂ）の段階では配線層数は２つになる。）。また、外側に積層する配線板素材１ａ、１ｂは、必ずしも、図５（ｂ）に示すように導電性バンプ４１ａ（４２ａ）を伴っていなくてもよい。この場合、導電性バンプ４１ａ（４２ａ）がないので、銅箔２１ａ（２４ａ）と配線層２２（２３）との層間接続は、導電性バンプによって行なうことはできないが、積層後の配線板にスルーホールを設けこのスルーホールによる層間接続構造を形成することはできる。

【0051】

外側に位置すべき絶縁層をコア配線板４と積層・一体化したら、次に、図６（ｃ）に示すように、両外側の銅箔２１ａ、２４ａに対してパターニングを施し配線層２１、２４を形成する。このパターニングは、図３（ａ１）、（ａ２）を参照した配線層２２、２３の形成工程と同様に行なうことができる。すなわち、化学研磨、レジスト用ドライフィルム積層、フォトマスクを介する露光、現像、エッチングという手順である。なお、以上の外側絶縁層１１、１４の積層、配線層２１、２４の形成のあと、さらにこの外側に同様の要領により絶縁層と銅箔とを積層・一体化（ビルドアップ）してもよい。

【0052】

次に、図６（ｃ）に示すように、最外側面の所定の位置に半田レジスト３１、３２を形成する。さらに、配線層２１または２４の半田レジストの形成されない部位には腐蝕防止のため無電解めっき法によりニッケル／金（ニッケルが下地）の層（図示せず）を形成する。そして、配線板をルータ加工機により所定の外形となるように切り出す。以上により

本実施形態に係る部品内蔵配線板を得ることができる。

【0053】

この実施形態では、製造設備として既存のものをほとんどそのまま使用することができ、配線板の製造コストの抑制につながる。また、最外の配線層２１、２４下の層間接続に導電性バンプ４１、４２を用いたので配線長を短くし電気的特性を向上して効率的に配線板としてレイアウトができる。また、比較的実装点数が多くなるチップ抵抗、チップコンデンサを内蔵できるので、現行設計ルールの緩和および一層の高密度実装が可能である。さらに、部品３３をマウント・内蔵するための工程では、部品マウントでの不良発生が極めて小さく歩留まりのよい製造が可能である。加えて、内蔵された部品３３の周りを絶縁層１１、１４が覆うように密着し、空隙の発生を防止するので信頼性の向上がなされる。

【0054】

次に、本発明の別の実施形態に係る部品内蔵配線板について図７を参照して説明する。図７は、本発明の別の実施形態に係る部品内蔵配線板の模式的な構成を示す断面図である。図７において、すでに図１ないし図６において説明したものと同一の部位には同一の符合を付してある。以下重複を避けて説明する。

【0055】

この実施形態では、内側積層の絶縁層１２、１３に代えて絶縁層１５、１６、１７を用い、それらの境界付近には配線層２５、２６が設けられている。また、配線層２２、２３と配線層２５、２６の４層でもそれらの隣接する配線層間の層間接続には導電性バンプ４３、４４、４５が用いられている。部品３３が半田３６、３７を介して接続される導電層３４、３５は、内側の配線層２５、２６とも直接的な電気的接続が可能となっている。なお、導電性バンプ４３、４４、４５は、その製造工程として例えば図５で説明したようなスクリーン印刷を用いて形成することができる。

【0056】

この実施形態の利点は、部品３３を内蔵するためのコア配線板の総厚（絶縁層１５、１６、１７の総厚：例えば０．２ｍｍ）に対して、３つの導電性バンプ４３、４４、４５で層間接続を行うことにより、すべての層間接続を導電性バンプによりなすようにしたことである。ここで、コア配線板を３つの導電性バンプ４３、４４、４５により層間接続したのは、これより数が少ない場合には高いバンプ形成が必要となり効率的な導電性バンプの形成が難しいからである。このように３つ程度とすれば、０．２ｍｍ程度の総厚に対して必要な形成高さにはさほどの困難さは生じない。この結果、コア配線板は４層の配線層となり、全体として６層の配線層となっている。

【0057】

ただし、導電性バンプ４３、４４、４５の形成高さをより高くすればより厚いプリプレグを貫通させることが可能であり、この結果、同じ部品３３を内蔵するとしてもコア配線板の配線層の数を少なくすることができる。逆に、導電性バンプ４３、４４、４５の形成高さをより低くすればより薄いプリプレグを用いることになり、この結果コア配線板の配線層の数を多くすることができる。

【0058】

図７に示す部品内蔵配線板を製造するには、図２（ａ）に示した両面銅張り板に代えて、絶縁板１５、１６、１７、銅箔２２ａ、２３ａ、配線層２５、２６、導電性バンプ４３、４４、４５を構成要素とする４層板を用いればよい。その後のプロセスは図２から図６に示したものと本質的に同様である。４層板を得るには、導電性バンプの印刷・形成、形成された導電性バンプにプリプレグを貫通（以上は図５を参照できる。）、貫通後に対向する側に銅箔（または配線層付きの絶縁層）を積層、というプロセスを繰り返せばよい。

【0059】

この実施形態では、先の実施形態と同様に製造設備として既存のものをほとんどそのまま使用することができ、配線板の製造コストの抑制につながる。また、部品３３をマウント・内蔵するための工程では部品マウントでの不良発生が極めて小さく歩留まりのよい製造が可能であることも同様である。さらに、コア配線板における配線層を４つとすること

により、コア配線板の厚さを部品内蔵空間が確保しやすい寸法とし、配線層同士の層間接続をすべて導電性バンプ４１～４５で行うことにより一層の高密度実装を実現することが可能である。

【図面の簡単な説明】

【0060】

【図1】本発明の一実施形態に係る部品内蔵配線板の模式的な構成を示す断面図および一部平面図。

【図2】本発明の一実施形態に係る部品内蔵配線板を製造するプロセスを模式的に断面（または一部平面）にて示す図。

【図3】図２の続図であって、本発明の一実施形態に係る部品内蔵配線板を製造するプロセスを模式的に断面（または一部平面）にて示す図。

【図4】図３の続図であって、本発明の一実施形態に係る部品内蔵配線板を製造するプロセスを模式的に断面（または一部平面）にて示す図。

【図5】本発明の一実施形態に係る部品内蔵配線板の製造に必要な配線板素材の構成を模式的に断面にて示す図。

【図6】図４の続図であって、本発明の一実施形態に係る部品内蔵配線板を製造するプロセスを模式的に断面にて示す図。

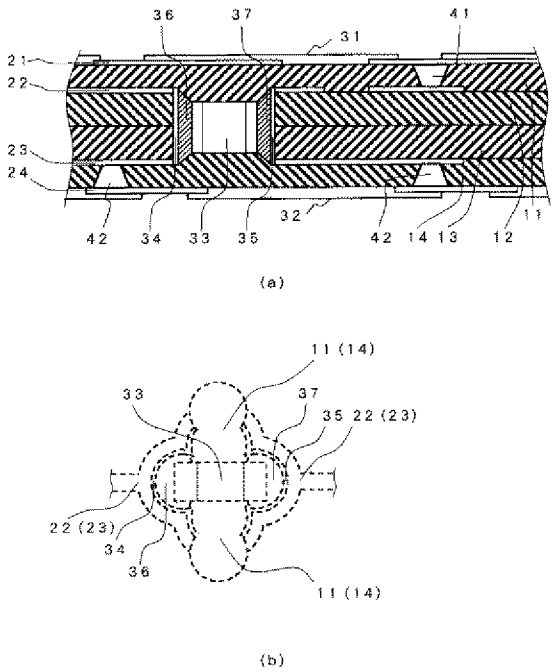
【図7】本発明の別の実施形態に係る部品内蔵配線板の模式的な構成を示す断面図。

【符号の説明】

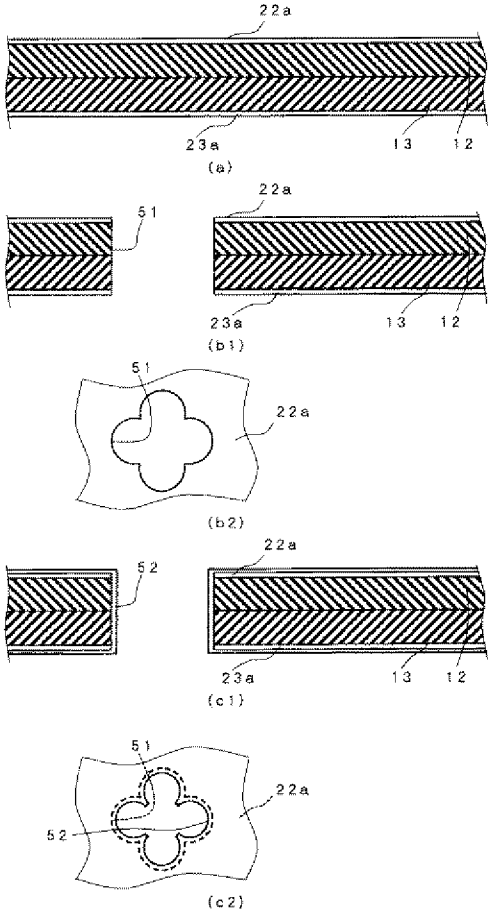
【0061】

１ａ、１ｂ…配線板素材、４…配線板素材（コア配線板）、１１、１２、１３、１４、１５、１６、１７…絶縁層、２１、２２、２３、２４、２５、２６…配線層、２１ａ、２２ａ、２３ａ、２４ａ…銅箔、３１、３２…半田レジスト、３３…電気／電子部品、３４、３５…導電層、３６、３７…半田、３６ａ、３７ａ…クリーム半田、４１、４２、４３、４４、４５…導電性バンプ（接続形成後）、４１ａ、４２ａ…導電性バンプ（接続形成前）、５１…貫通孔、５２…めっき層、５３…めっき層分断貫通孔、５３Ａ…バリ、６１…支持部材、６１ａ…粘着層。

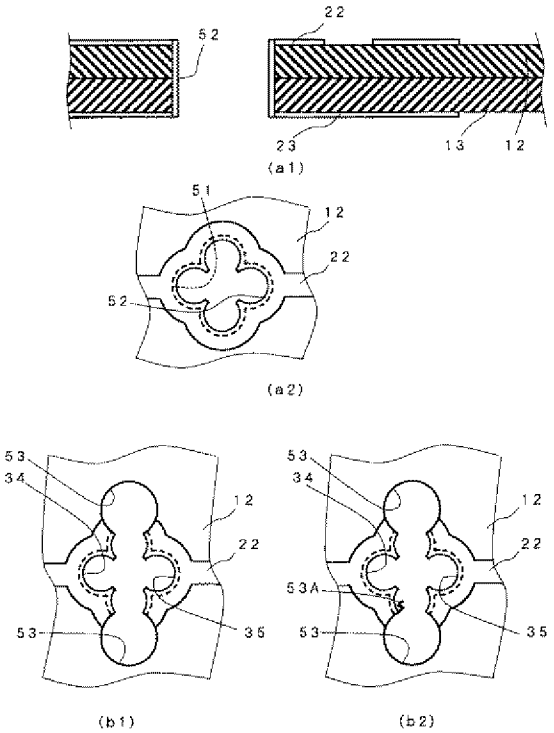
【図1】


36
37
31
41
21
22
23
24
42
34
33
35
32
42
14
13
12
11
(a)
11 (14)
33
37
35
22 (23)
22 (23)
34
36
11 (14)
(b)

【図2】


22a
23a
13
12
(a)
51
22a
23a
13
12
(b1)
51
22a
(b2)
52
22a
23a
13
12
(c1)
51
22a
52
(c2)

【図3】


52
22
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13
12
(a1)
51
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(a2)
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(b1)
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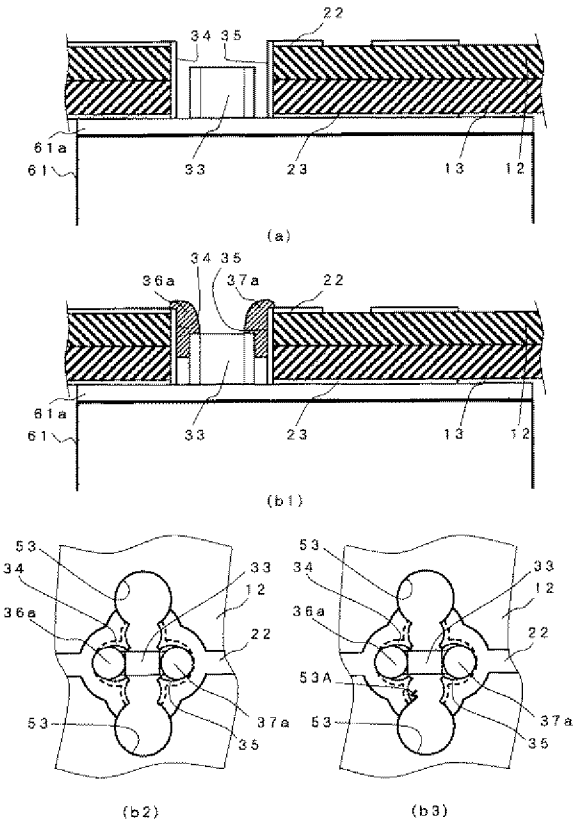
34
12
22
53A
53
35
(b2)

【図4】


34
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61a
61
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12
(a)
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36a
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22
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61
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23
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36a
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37a
35
(b2)
53
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33
12
36a
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53A
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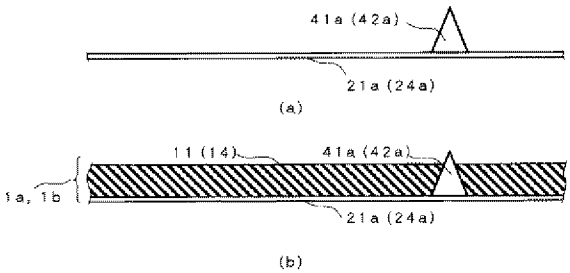
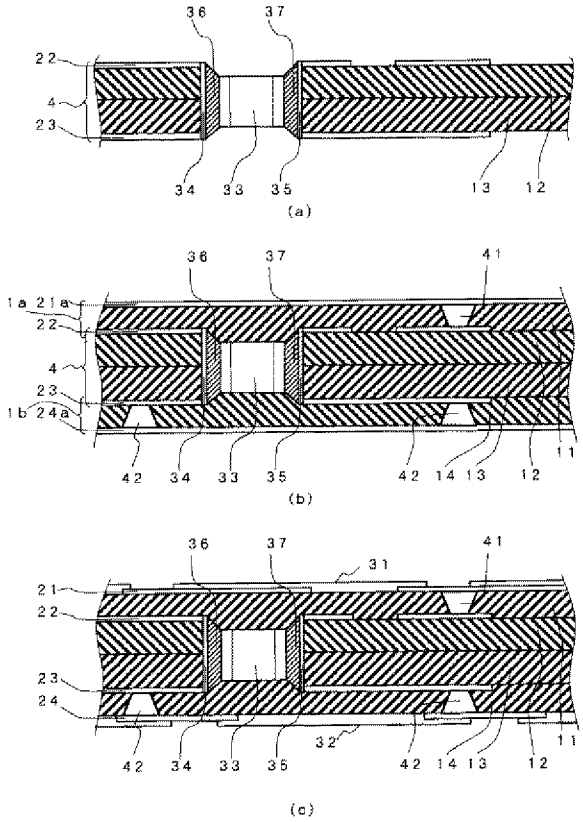
37a
35
(b3)

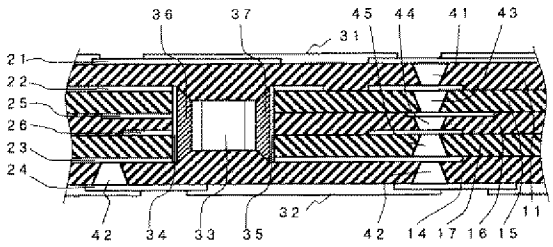
【図5】


41a (42a)
21a (24a)
(a)
11 (14)
41a (42a)
1a, 1b
21a (24a)
(b)

【図6】


36
37
22
4
23
34
33
35
13
12
(a)
41
1a 21a
1b 24a
11
42
14
(b)
31
21
24
32
(c)

【図7】


36
37
45
44
41
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31
21
22
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23
24
32
42
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14
17
16
15
11

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